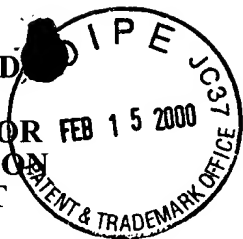


FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT
 Applicant:
 Case:
 Serial No.:
 Filing Date:
 Group:

 K. Azadet, E.F. Haratsch #3
 10-2
 09/471,920
 December 23, 1999
 2739 2631

U.S. PATENT DOCUMENTS

EXAMINER				FILING DATE	
INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER				TRANSLATION	
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OTHER DOCUMENTS

EXAMINER		REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
INITIAL			

- | | | |
|-----------|----|---|
| <i>HA</i> | 1. | Fettweis et al., "High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture," IEEE Communications Magazine, May 1991. |
| <i>HA</i> | 2. | Chevillat et al., "Decoding of Trellis-Encoded Signals in the Presence of Intersymbol Interference and Noise," IEEE Transactions on Communications, Vol. 37, No. 7, July 1989. |
| <i>HA</i> | 3. | Erich F. Haratsch, "High-Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000Base-T," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA. |
| <i>HA</i> | 4. | K. Azadet, "Gigabit Ethernet over Unshielded Twisted Pair Cables," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA. |
| <i>HA</i> | 5. | Black et al., "A 140-Mb/s, 32-State, Radix-4 Viterbi Decoder," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, December 1992. |
| <i>HA</i> | 6. | Cypher et al. "Generalized Trace-Back Techniques for Survivor Memory Management in the Viterbi Algorithm*," Journal of VLSI Signal Processing, 5, 85-94(1993). |

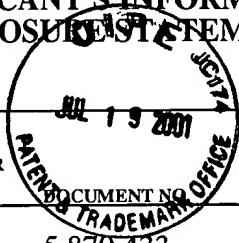
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#5



U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
<i>HP</i>	5,870,433	2/9/99	Huber et al.		
<i>HY</i>	6,035,006	3/7/00	Matui		
<i>MM</i>	6,201,831	3/13/01	Agazzi et al.		

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
<i>HP</i>	1.	Keshab K. Parhi, "Pipelining in Algorithms with Quantizer Loops," IEEE Transactions on Circuits and Systems, Vol. 38. No. 7, 745-754 (July 1991)
<i>MM</i>	2.	Bednarz et al., "Design, Performance, and Extensions of the RAM-DFE Architecture," IEEE Transactions on Magnetics, Vol. 31, No. 2, 1196-1201 (March 1995)

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